Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1-8. (Cancelled).

9. (Previously Presented) A method of measuring an input signal using a single-ended sense amplifier, the method comprising:

sampling a voltage present at an input node a predetermined interval before measurement of the input signal is initiated;

holding the sampled voltage at a reference node as a reference voltage; and

at the predetermined interval after sampling the voltage present at the input node, measuring the input signal at the input node by sampling the input signal and comparing it to the reference voltage.

10. (Previously Presented) The method of claim 9 wherein sampling the voltage present at the input node comprises activating a sampling circuit a predetermined interval before measurement of the input signal is initiated.

11. (New) The method of claim 9 wherein the single-ended sense amplifier is part of a global sense amplifier to sense the input signal.

12. (New) The method of claim 9 wherein an output signal of the single-ended amplifier is used in a feedback path to adjust the reference voltage.

13. (New) The method of claim 9 wherein the output signal of the single-ended amplifier is used in a feedback path to adjust the reference voltage by capacitive coupling.

14. (New) The method of claim 13 wherein the feedback path is used to adjust amplifier gain.

15. (New) The method of claim 12 wherein the feedback path is coupled to a source and a drain of a transistor, and wherein the source of the transistor is coupled to the drain of the transistor.

16. (New) The method of claim 15 wherein a gate of the transistor is coupled to the reference node.

17. (New) The method of claim 9 wherein the reference node is coupled to a transistor that is configured to add capacitance to the reference node.

18. (New) The method of claim 17 wherein the transistor is configured to pump capacitance to compensate for a voltage decrease at the reference node in response to an activate signal.

19. (New) The method of claim 18 wherein the activate signal is asserted to activate a sampling circuit that samples the voltage present at the input node.

20. (New) The method of claim 18 wherein the activate signal is input at a second input node of the single-ended sense amplifier.

21. (New) The method of claim 9 wherein the single-ended sense amplifier is part of a memory structure.

22. (New) The method of claim 21 wherein the memory structure comprises a hierarchical memory structure.

23. (New) The method of claim 21 wherein the memory structure employs redundant memory modules that can be mapped to failed memory circuits.

24. (New) The method of claim 21 wherein the memory structure employs one or more redundant rows or columns that can be mapped to one or more failed rows or columns of the memory structure.

25. (New) The method of claim 21 wherein the memory structure employs voltage-swing reduction techniques.

26. (New) The method of claim 25 wherein the voltage-swing reduction techniques reduce power dissipated as a voltage at a particular node or on a particular line of the memory structure decays during a particular event or a particular operation.

27. (New) The method of claim 9 wherein the single-ended sense amplifier is part of an SRAM memory structure.

28. (New) The method of claim 9 wherein the single-ended sense amplifier is part of a VLSI memory subsystem.